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LOGIC AND CIRCUIT CONSIDERATIONS IN THE DESIGN OF A DIGITAL DIFFERENTIAL ANALYZER TO BE USED AS A TEST TOOL FOR EVALUATION OF ADVANCED MEMORY DEVICES

16 January 1963

U S ARMY MISSILE COMMAND
REDSTONE ARSENAL, ALABAMA

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LOGIC AND CIRCUIT CONSIDERATIONS IN THE DESIGN OF A DIGITAL DIFFERENTIAL ANALYZER TO BE USED AS A TEST TOOL FOR EVALUATION OF ADVANCED MEMORY DEVICES

by

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Department of the Army Project No. 516-01-004
Army Materiel Command Management Structure Code No. 5221.11.146

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ABSTRACT

This report deals with the technical design and problems encountered in the building of a Digital Differential Analyzer (DDA), a test tool for evaluation of advanced memory devices, digital to analog and analog to digital converters. The first step in building the test tool was to select a particular guidance scheme to mechanize. The Pershing Missile Guidance was instrumented for this purpose. In order to simplify the building of the DDA commercial digital modules were used as the basic components.

The logical design, construction, and testing of all the circuits were completed, and all units operated satisfactorily. In order to make accuracy tests with actual acceleration profiles it was necessary to construct a device to serve as a buffer between the DDA and a general purpose digital machine which would provice the proper input data.

Upon completion of the DDA test tool, evaluation work on advanced memory systems and input-output devices will be started. Reports on this subject will be prepared at the conclusion of the work.

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SYMBOLS

Vo - initial preset velocity
Vm - measured velocity
Do - initial preset displacement
Dm - measured displacement
T - preset time constant
t - portion of T stored in normal register
tx - portion of T stored in bits supplementing normal register
dt - calculation period of the computer; equal to one word time in original concept and equal to four word times in time-shared concept
Fw - time share control flip flop
tx contr - tx control; the logic required to operate upon tx
slot gate - a gate which is true during any particular bit time and used to help generate discrete pulses.
discrete pulse - any one of four pulses during a particular bit, which repeats only once per word time.
sequencer - timing pulse generator for synchronization purposes
1 -increm adder - one increment adder, adds a single bit to a full binary word
2 -increment adder - adds two bits to a binary word in one bit position

Pulse numbering scheme: the subscript denotes the pulse within a bit, and the number in parentheses denotes the particular bit. Example: $t_3(12)$ represents the third pulse during the twelfth bit.

I. INTRODUCTION

This report contains the detailed technical design of a DDA computing device designed for use as a testing tool in the evaluation of new memories and converters. The work was performed under the 1962 Supporting Research project.

The 1962 Supporting Research program on Digital Guidance and Control techniques was directed toward development of advanced memory devices, digital to analog and analog to digital converters. These new devices must have the potential of high reliability, low cost, and must be compatible with the Army's future computing systems. In order to determine feasibility and compatibility it was decided to build a small DDA computer to simulate a guidance system, then use the DDA as a test tool for evaluation of the new designs operating in the computer systems environment.

This report deals with the technical design and problems encountered in the building of the test tool. Reports on the new memory and converting devices will be written at the completion of their evaluation. The first step in building the test tool was to select a particular Guidance Scheme to mechanize; since this laboratory has intimate knowledge of the Pershing Guidance system, it was decided to instrument this scheme using DDA techniques. This gives us a test tool to be used in evaluating the new memories and converter and at the same time strengthens the in-house capabilities in the digital computer field. In order to simplify the building of the test tool commercial digital modules were used as the basic components and the logic design and fabrication was accomplished in the laboratory.

II. TECHNICAL DISCUSSION - DDA

The Digital Differential Analyzer was designed to implement the Pershing slant range equation, with the intention to add lateral channel computations at a later date. The form of the equation chosen is $(-\bar{V}o\bar{T} + \bar{V}m\bar{T}) + (Do - \bar{D}m) = 0$ where $-\bar{V}o$, Do and $\bar{T}$ are preset parameters representing initial velocity, initial displacement, and a time function respectively, and $\bar{V}m$ and $\bar{D}m$ are the values of missile velocity and displacement measured during flight. The measured displacement is obtained by a single integration of velocity terms: $\bar{D}m = \int_0^t (Vm - Vo)\, dt$. The cut-off signal is generated by preloading a register with the calculated presettings $(-\bar{V}o\bar{T} + Do)$ and then adding to this term increments of $(+\bar{T}\,\Delta\,\bar{V}m)$ and $(-\,\Delta\,\bar{D}m)$ until the register is driven to zero.

The block diagram in Fig. 1 shows the signal flow paths between five shift registers and five adder and gate units comprising the original computer configuration. Briefly, the computer receives velocity increments ($\Delta\,\bar{V}m$) from an accelerometer and sums them with ($-Vo$). The result ($\bar{V}m - Vo$) is then integrated to produce increments of displacement ($\Delta\,\bar{D}m$). Simultaneously, the $\Delta\bar{V}m$'s are multiplied by the constant $\bar{T}$ and summed, resulting in the accumulation of $\bar{V}m\bar{T}$. When the $\bar{V}m\bar{T}$ register overflows the resulting $\Delta\,\bar{V}m\bar{T}$'s and the $\Delta\,\bar{D}m$'s produced by the integration are summed with the pre-selected value of $(-\bar{V}o\bar{T} + Do)$ to solve the cut-off equation.

The present configuration of the computer is shown in Fig. 2. The basic calculation process is the same as before with the same results. The primary difference in the two schemes is that now one full adder is time-shared, which has eliminated the $\bar{V}m\bar{T}$ register and its associated full adder If the circuit cards being used had a higher speed capability it would be possible to use only one adder to perform all the additions required by the computer with a subsequent saving in components.

Construction is being carried out using digital modules of the printed circuit card form purchased from the Packard-Bell Computer Corporation. Magnetic cores are used for each of the registers, and the various adders, gates and control circuits utilize flip flops, diode gates and pulse amplifiers. In the future the magnetic core registers will be replaced by magnetic thin film registers in continuing support of advanced techniques.

The computer is based on an 18-bit word using one bit for sign indication and a basic clock frequency of 200 kc. The shifting rate per bit is 100 kc which results in a word time of 180 usec. The velocity term $(Vm - Vo)$ is integrated every fourth word time resulting in an integration period of 720 usec.

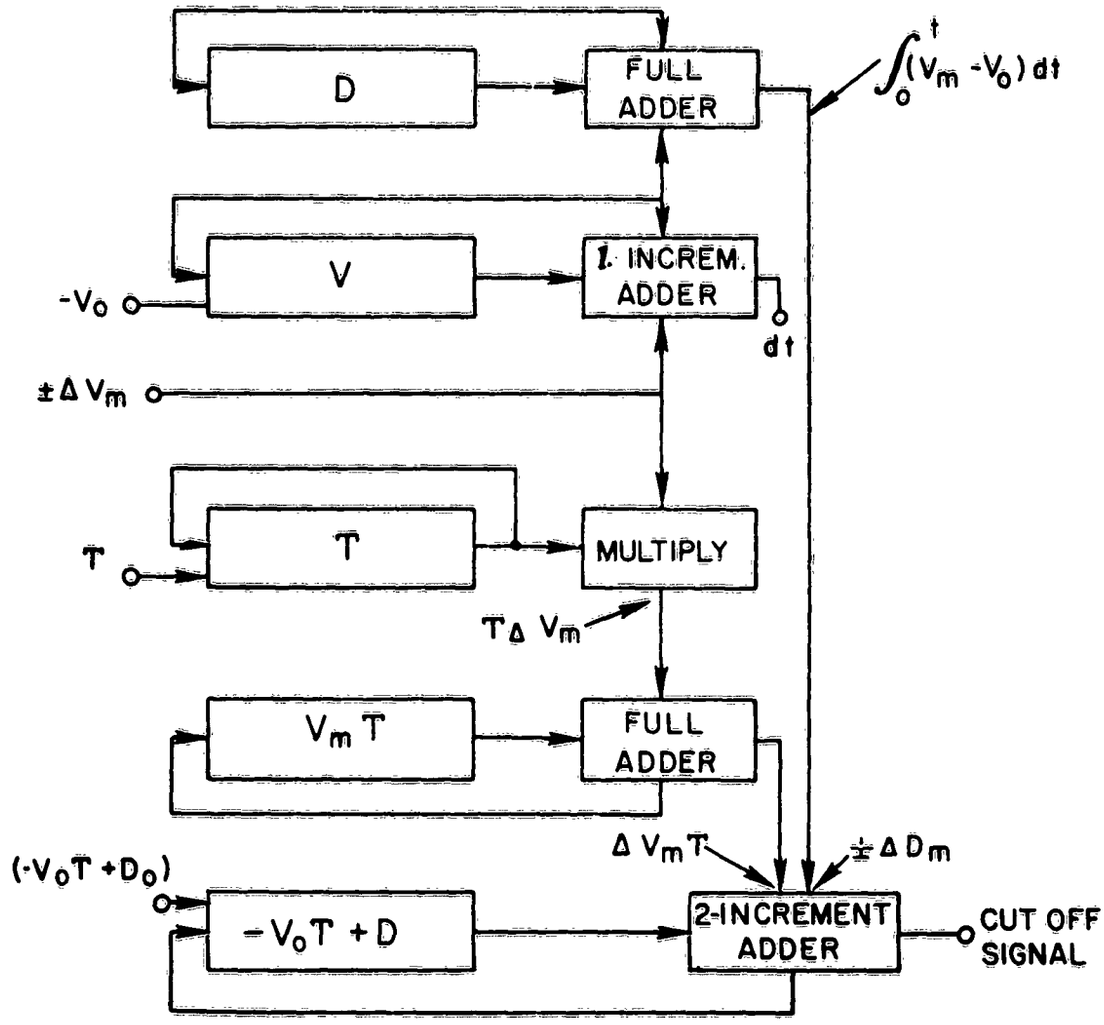


Figure 1. BLOCK DIAGRAM ORIGINAL

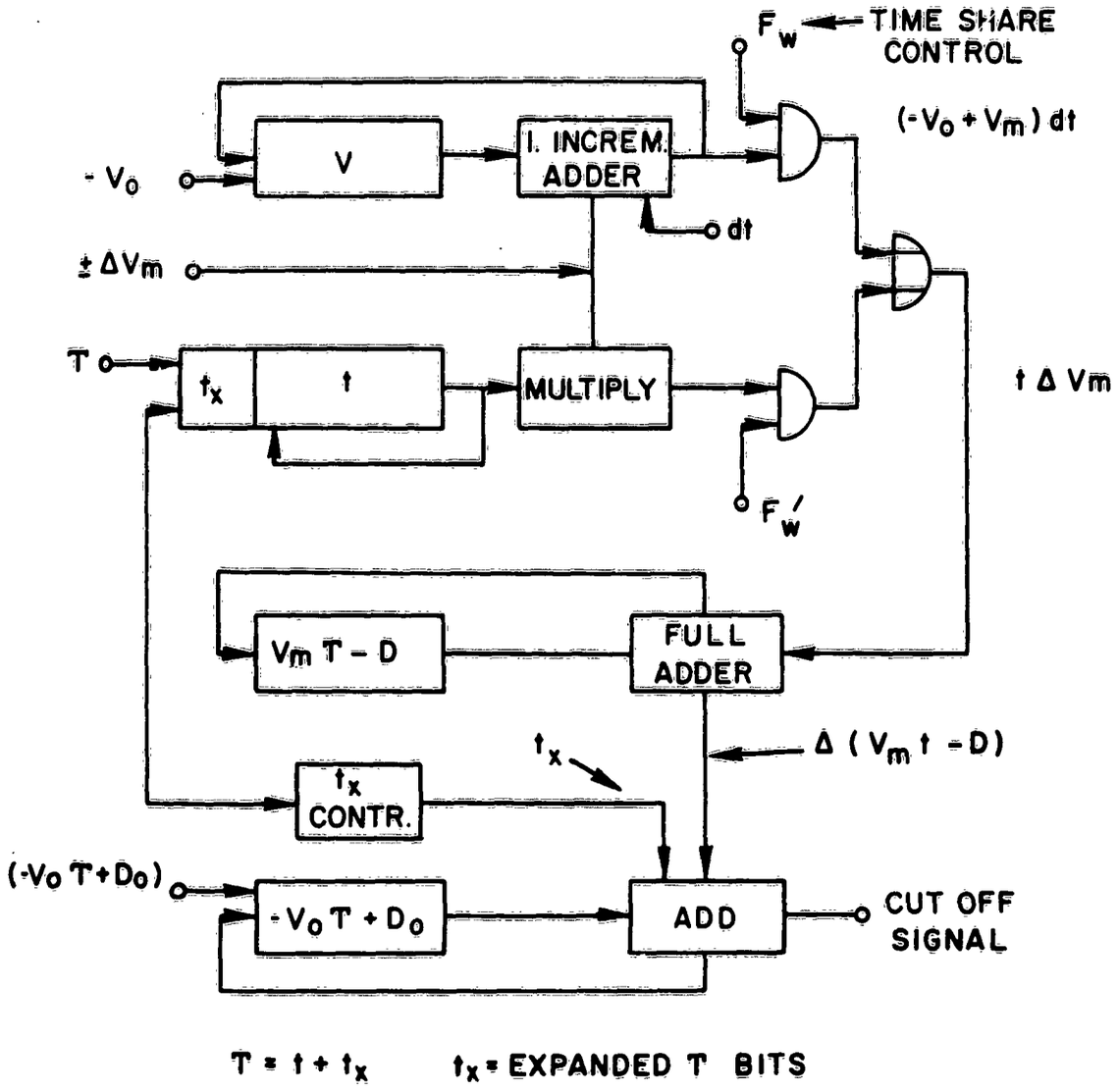


Figure 2. BLOCK DIAGRAM TIME SHARED REVISION

Due to the type of equation used, resulting in a displacement solution rather than one in velocity, the maximum and minimum values of T depend upon the resolution of the velocity increments, the calculation period and the weight of $\bar{T}\Delta\bar{V}m$ with respect to $\Delta\bar{D}m$. For maximum accuracy $\bar{T}\Delta\bar{V}m$ should be equal to $\Delta\bar{D}m$. This requirement leads to a difficulty in scaling T. The maximum $\bar{1}$ that is possible using seventeen bits (one bit reserved for sign) turns out to be too small.

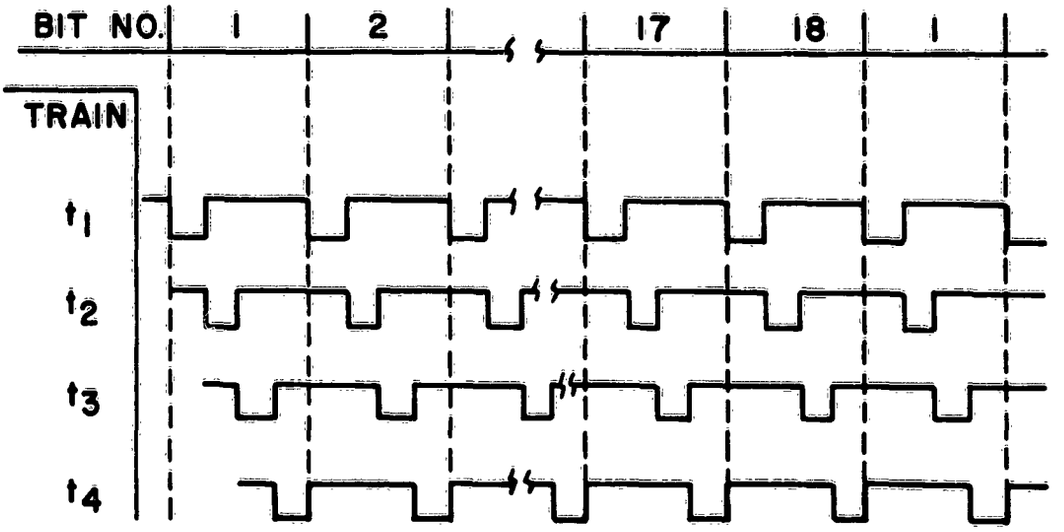
The problem was attacked from several viewpoints. One proposed solution would have scaled $\bar{T}$ max to a larger value at the expense of reduced cut-off accuracy. It soon became evident that any increase in $\bar{T}$ max would result in a corresponding decrease in cut-off accuracy unless the size of the $\bar{T}$ register was enlarged.

A maximum T can be easily scaled if the T register has 22 bits of information, an increase of 4 bits over the normal word length of 18 bits where one bit is reserved for sign indication. These extra bits will be provided by splitting the $\bar{T}$ register so that the first four bits are scaled to represent values equivalent to bits eighteen through twenty-three of a longer register. When any of the additional bits are present they will be inserted directly into the $(-V_o\bar{T} + \bar{D}o)$ register at the proper time. Additional logic is required to process the expanded $\bar{T}$ function, but it is felt that the expenditure of components to buy more than an order of magnitude of accuracy is justified. The need to expand T gave impetus to the decision to time-share the full adder, as a time-sharing scheme makes it easier to mechanize the insertion of the excess T bits.

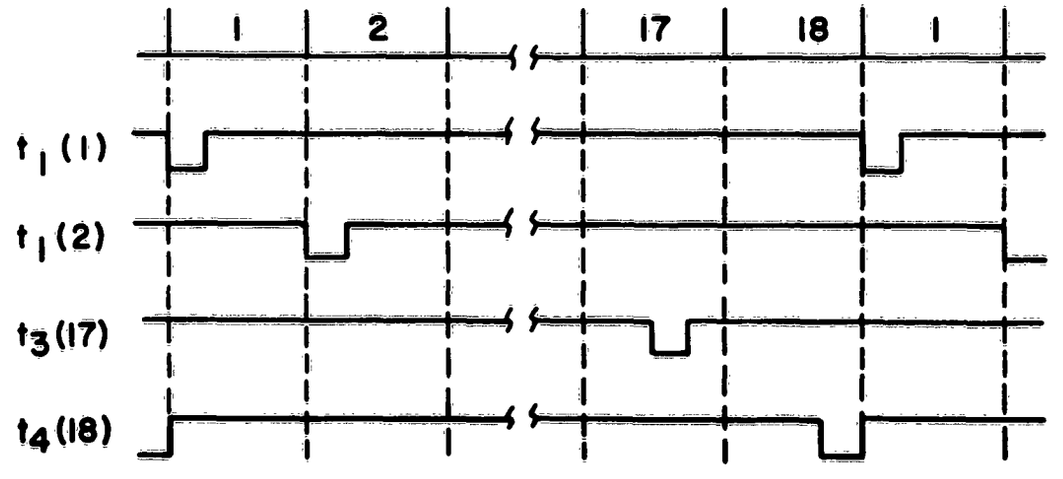
The heart of any digital computer is the synchronizing device. We have chosen to label the synchronizing device for the DDA as a sequencer. The sequencer generates all the timing pulses which are required to perform arithmetic operations in the computer as well as synchronizing the data inputs and time-sharing functions.

Three types of pulses are generated by the sequencer. First, four pulse trains shifted 90° in phase from each other provide the functions of register shifting and basic arithmetic operations. Second, discrete pulses within the pulse trains provide start, stop and panel light readout synchronization, data input synchronization and special arithmetic operations such as positive or negative register overflow outputs and processing expanded T bits. Third, a flip flop Fw is pulsed every word time to provide the time-sharing control function. Fig. 3 depicts the three types of pulses. Each train is 18 pulses long, and each bit can be operated upon by four separete pulses, one from each train. A logically switched binary counter is used in conjunction with the pulse trains to obtain the discrete pulses.

a. PULSE TRAINS



b. DISCRETE PULSES



c. TIME SHARE CONTROL F w

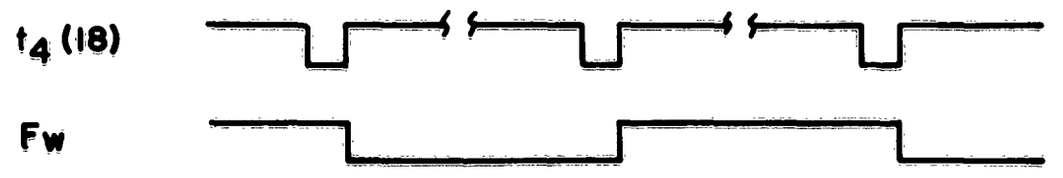


Figure 3.

Several problems have arisen relative to time-sharing the full adder. Most of the difficulties are directly related to the increased clock speed necessary to maintain accuracy when time-sharing two addition functions. The register shifting speed had to be increased from 50 kc to 100 kc. As the maximum clock frequency is determined by the modules used, the sequencer was redesigned to obtain four 100 kc pulse trains from the maximum clock frequency of 200 kc. Other problems relative to the modules are presented later.

With a maximum clock capability of 200 kc it was decided to achieve the four pulse trains by dividing the clock C by two with a flip flop. The flip flop outputs (C/2) and (C/2)' are then combined with the clock and an inverted clock C' to produce the required phasing. (See Fig. 4).

An eighteen-bit binary counter triggered from one of the four pulse trains is the basic unit of the sequencer. In the beginning it was composed of toggle-input flip flops. Five stages were required and the counter must be reset in mid-cycle as a full cycle represents a count of thirty-two. In trying to build slot gates for bits 17 and 18 it was noted that an extra pulse appeared with t_1 (17 and 18) and t_3 (17 and 18). This was traced to a 3.5 usec. propagation delay in the counter at reset because each of the five flip flops had to change state in sequence. The delay of a single flip flop was measured and found to be over 0.5 usec using toggle inputs and approximately 0.2 usec using set-reset inputs. The obvious solution was a logically switched counter in which only one flip flop changes state for any single count. This reduces the propagation delay to the minimum possible value. It also requires, however, extra gating for each set and reset input of the counter.

The present counter is switched according to a cyclic code which was derived with the use of a diagram representing four control gates and the states of four counting flip flops. The count sequence is shown in Fig. 5. The slot gates are now generated using the count and control gate outputs.

The sequencer has been completed and operates very satisfactorily. All discrete pulses are clear and well defined. Fig. 6 shows some photographs taken of some of the actual voltage wave shapes present in the sequencer and one picture describing the time sharing function. Fig. 6 (a) depicts the four timing pulse trains, and Fig. 6 (b) shows t_1, t_2, t_3, t_4, and a slot gate for one particular bit. In Fig. 6 (c) a pulse train and a slot gate are combined to give a discrete pulse output, in this case $t_1(1)$. The first trace in Fig. 6 (d) shows $t_1(1)$ recurring every 18 bits while the second trace is the time-share flip flop Fw as it changes every 18 bits. Traces three and four are on a different time base from one and two.

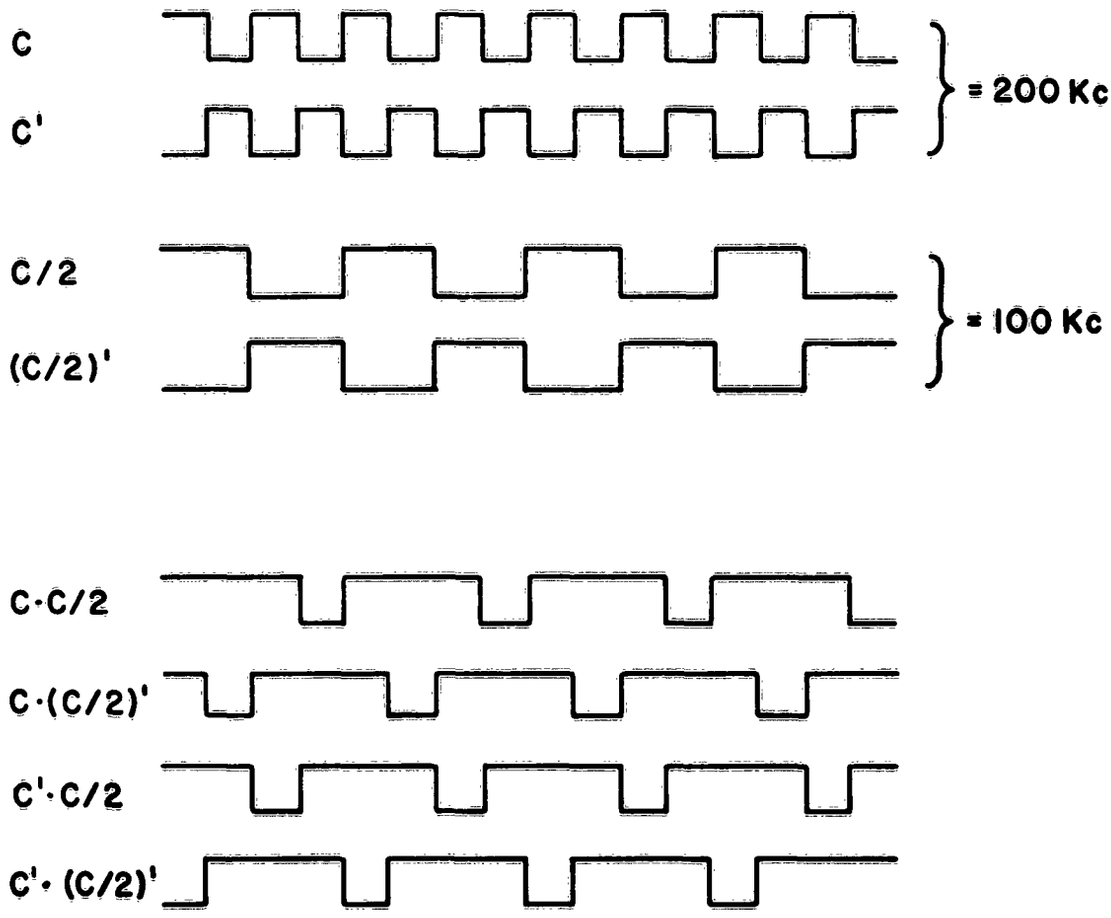
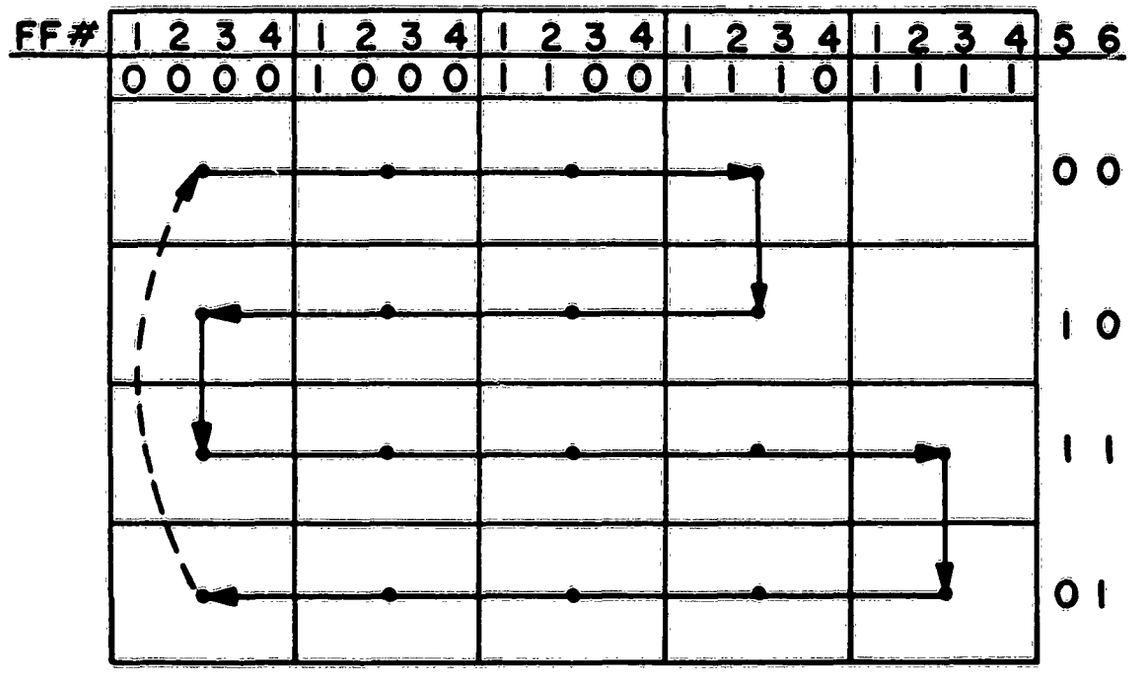


Figure 4. GENERATION OF FOUR PULSE TRAINS FROM 200 KC CLOCK



FF # 1-4 = COUNTER
FF # 5&6 = CONTROL GATE INPUTS

COUNT BEGINS AT 1= 0000 00
COUNT ENDS AT 18= 0000 01 AND RESETS TO 1

⟶ = COUNT CYCLE
⟶ = RESET

Figure 5. COUNTER CYCLE CODE

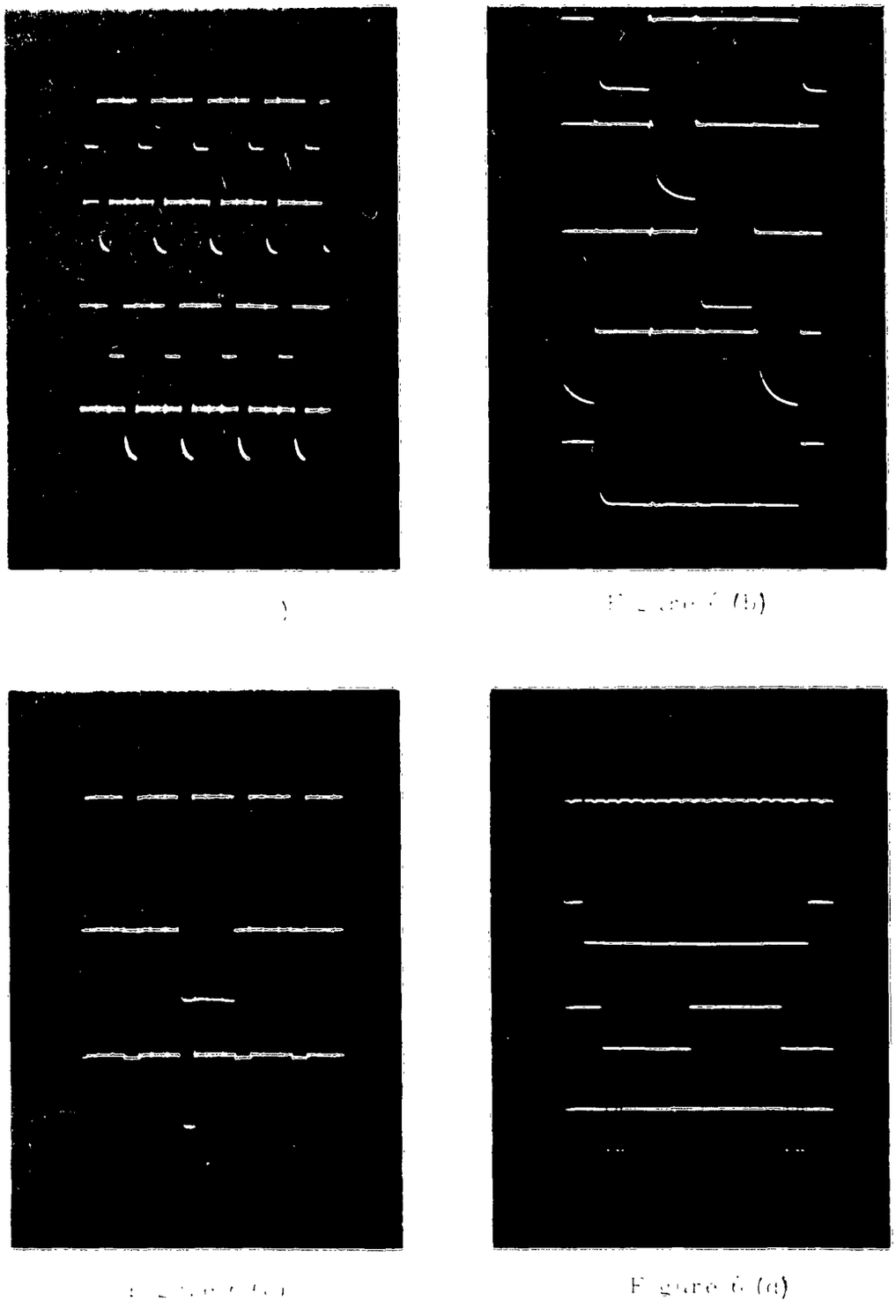


FIGURE 6 PHOTOGRAPHS OF ACTUAL VOLTAGE WAVE SHAPES AND TIME SHARING FUNCTION

Trace three is Fw once more, and trace four is one input to the time-shared adder, shown occurring every other word time.

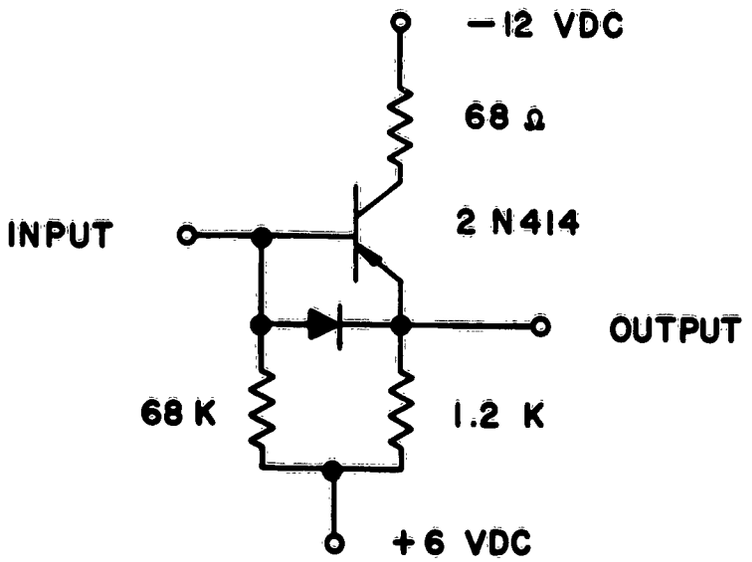
In working with the Packard-Bell logic cards several deficiencies have been noted. Some of these are due to the nature of the DDA, i.e., to the gate configurations mentioned above, the logic for the various adders and some of the control functions contains a good number of two input "and" gates. In order to mechanize such two-input gates it is necessary to waste a number of diodes on each card. In some cases it is impossible to utilize the extra diodes with other gates of three or four input terms. The relatively large number of two-input gates prompted the logical modification of one type of card in order to waste as few diodes as possible.

A problem arises in trying to set up DC "or" gates. The manner in which this is recommended by Packard-Bell requires the use of two types of cards - an "and" circuit coupled to an emitter follower. If it becomes necessary to drive more than three other gates with the "or" output, however, then an additional amplifier must be used. Therefore an "or" gate which must drive up to five "and" gates requires the use of at least three separate cards. In one particular case of the full adder a five term "or" is required. Rather than use the three cards normally required, one of the "and" gates was modified so that half of it was a five term "or" gate, thereby utilizing every diode on the card.

A lack of gate versatility for a particular system could be predicted when general purpose logic cards are used. One must also expect a certain amount of pulse shaping for gate driving purposes in this situation. There is one basic fault with the Packard-Bell system of so-called "building-block" logic cards which demands use of extra components. There is no circuitry provided in the complete line of cards which will allow the output of an "and or "or" gate or even a flip flop to set a binary 1 into one of the magnetic core registers. It is possible to build register recirculation loops with little or no difficulty, but if the output of an adder must be used to store information in a core, one quickly sees that it is impossible with a standard card. To circumvent this difficulty it became necessary to modify still another card to provide the core setting function. To see how an emitter follower circuit was modified for this purpose refer to Fig. 7.

Lesser problems stemming from the magnetic cores include the fact that the voltage outputs of the cores are positive-going spikes approximately -12 v dc to -4 v dc in amplitude. As -12 v dc to -8 v dc represents a logical "one", it is not possible to drive gates directly from the core outputs. The information can be stored in flip flops, however, and is in fact processed in this manner. Another minor problem related to the cores concerns the core driver card which provides a one ampere, two micro-second current pulse

a. EMITTER FOLLOWER



b. CORE INPUT DRIVER

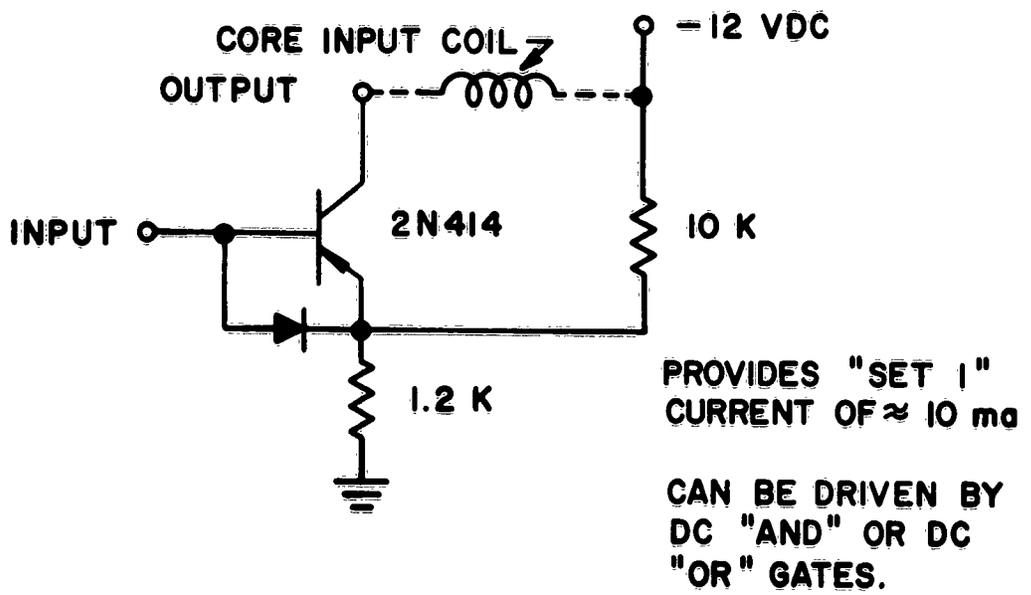


Figure 7. MODIFICATION OF EMITTER FOLLOWER TO CORE INPUT DRIVER

to the shifting line. At speeds near the specification maximum of 100 kc the output power transistor tends to become hot enough to draw excessive current and damage a 2.7 ohm, 1 watt resistor. This necessitated the addition of an extra driver card to equalize the driven loads.

III. CONCLUSION

This report has presented a review of the technical problems which have arisen in the mechanization of a DDA using general purpose logic cards.

The logical design, construction and testing of all circuits have been completed with all units operating satisfactorily. In order to make accuracy tests with actual acceleration profiles it has become necessary to construct a device to serve as a buffer between the DDA and a general purpose digital machine which will provide the proper input data. The problems associated with the buffer will be solved as they become apparent.

With the completion of the DDA test tool we will start evaluation work on the advanced memory system, and input-output devices. The design of new input/output devices is being carried on "in-house". Designs to reduce circuit complexity and to operate at sufficient speeds so that one circuit can be time-shared for many input-output functions are the major avenue of investigation. Reports on this subject will be prepared at the conclusion of the work. The approach taken on new memory devices was to let a contract for a sample of thin film magnetic domain type memory. The thin film shift registers will replace the core registers in the test tool, and be evaluated as to signal to noise, peripheral circuit complexity, speed of operation, and capability with the existing computer system.

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